Mobile Intel® 945 Express Chipset Family

Specification Update

November 2007

Document Number: 309220-0011

Contents

Revision History

Revision	Description	Date
-001	Initial release	January 2006
-002	Component Marking Information updated	March 2006
-003	• Added information for Mobile Intel® 945GMS and Intel® 940GML Express Chipset family • Updated workaround for Erratum #9	April 2006
-004	• Added Erratum #11	May 2006
-005	• New Errata — Added new Errata #12 • Added Specification Change — Added 200 MHz Display Clock Support for 940GML • Added Documentation Change • Section on 6.2.16 C0DRC0- Channel 0 DRAM Controller Mode 0 [6:4] update	July 2006
-006	• New Errata — Added new Errata #13 • Specification Clarification — Clarification of TCO0/TCO1 Default Value • Documentation Changes • Replace the diagrams in Figure 19-10 & Figure 19-13	September 2006
-007	• Specification Clarification — Added DMA Transfer Completion for Latency Sensitive Devices	October 2006
-008	• Updated disclaimer information	March 2007
-009	• Added Intel® 945GME Express Chipset information	August 2007
-010	• Updated workaround information for Erratum 12	August 2007
-011	• Updated Errata 12 • Updated Specification Clarification 2 • Added Errata 14	November 2007

§

Preface

This document is an update to the specifications contained in the documents listed in the following *Affected Documents/Related Documents* table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected / Related Documents

Document Title	Document Number / Location
Mobile Intel® 945 Express Chipset Family Datasheet	309219-002

Nomenclature

Errata are design defects or errors. Errata may cause the Mobile Intel® 945 Express Chipset family's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

§

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed (G)MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

Number	Steppings	SKU	Plans	ERRATA
	A3			
1	X	GM/GME/PM/GT/GMS/ GML	No Fix	LOCK to Non-DRAM Memory Flag (Register C8, Bit 9) Is Getting Asserted
2	X	GM/GME/PM/GT	No Fix	False Detection of a PCIe* Endpoint While Operating in PCIe Low Power Mode
3	X	GM/GME/PM/GT	No Fix	System Memory Clocks Do Not Meet Certain JEDEC DDR2-667 DRAM Device Jitter Requirements
4	X	GM/GME/PM/GT/GMS/ GML	No Fix	Intermittent Failure to Detect DVI Display Device during System Boot
5	X	GM/GME/PM/GT/GMS/ GML	No Fix	DDR2 CLK to CKE Power-up Timing
6	X	GM/GME/PM/GT/GMS/ GML	No Fix	LVDS Panel Power Down Timing Violation during System Reset
7	X	GM/GME/PM/GT/GMS/ GML	No Fix	Hang/Blue-screen While Running 3D Workloads in Battery Mode
8	X	GM/GME/PM/GT/GMS/ GML	No Fix	Screen-corruption with Hardware VLD Enabled
9	X	GM/GME/PM/GT/GMS/ GML	No Fix	No Display on Monitor after Resume from the Device Power-Down State with Intel® Smart 2D Display Technology (Intel® S2DDT) Enabled
10	X	GM/GME/PM/GT/GMS/ GML	No Fix	CLK-CKE Hold Time Violation on DDR2
11	X	GM/GME/PM/GT/GMS/ GML	No Fix	Power Savings Optimization Erratum
12	x	GM/GME/PM/GT/GMS/ GML	No Fix	Mobile Intel 945GM/GME/945GMS/940GML Express Chipset Internal Buffer Logic Erratum
13	x	GM/GME/PM/GT/GMS/ GML	No Fix	Mobile Intel® 945 Express Chipset Family SMRAM D_CLS Bit Erratum
14	X	GM/GME/PM/GT/GMS/ GML	No Fix	Mobile Intel® 945 Express Chipset Family Internal Race Condition between the Host and PCI Express Internal Clocks

Number	SPECIFICATION CHANGES
1	Mobile Intel® 940GML Express Chipset Added Support for 200-MHz Display Clock

Number	SPECIFICATION CLARIFICATIONS
1	Clarification of TCO0/TCO1 Default Value
2	DMA Transfer Completion For Latency Sensitive Devices

Number	DOCUMENTATION CHANGES
1	Section 6.2.16 C0DRC0- Channel 0 DRAM Controller Mode 0 [6:4] update
2	Replaced Figure 37 and Figure 40 diagrams

Identification information

Component Identification via Programming Interface

The Mobile Intel® 945GM/GME/PM/GMS, 940GML Express Chipsets and Intel® 945GT Express Chipset steppings can be identified by the following register contents:

Product	Stepping	CRID[1]	Device ID[2]
Mobile Intel® 945GM Express Chipset (lead-free)	A3	03	27A0h
Mobile Intel® 945PM Express Chipset (lead-free)	A3	03	27A0h
Intel® 945GT Express Chipset (lead-free)	A3	03	27A0h
Mobile Intel® 940GML Express Chipset (lead-free)	A3	03	27A0h
Mobile Intel® 945GMS Express Chipset (lead-free)	A3	03	27A0h
Mobile Intel® 945GME Express Chipset (lead-free)	A3	03	27ACh

NOTES:

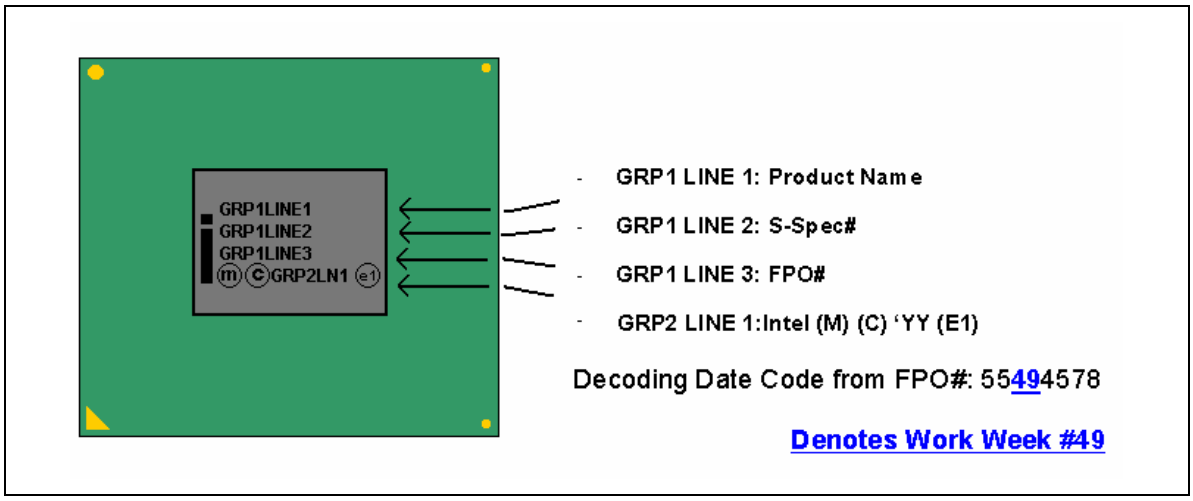
1. CRID can be determined by reading the register at Device 0, Function 0, Offset 08h.
2. Device ID can be determined by reading the register at Device 0, Function 0, Offset 02-03.

Component Marking Information

The Mobile Intel 945GM/GME/PM/GMS, 940GML Express Chipset and Intel 945GT Express Chipset may be identified by the following component markings:

Product	Stepping	MM#	S-SPEC
Mobile Intel® 945GM Express Chipset (lead-free)	A3	876956	S L8Z2
Mobile Intel® 945PM Express Chipset (lead-free)	A3	876959	S L8Z4
Intel® 945GT Express Chipset (lead-free)	A3	876960	S L8Z6
Mobile Intel® 940GML Express Chipset (lead-free)	A3	876958	S L8Z5
Mobile Intel® 945GMS Express Chipset (lead-free)	A3	876223	S L8TC
Mobile Intel® 945GME Express Chipset (lead-free)	A3	890229	S LA9H

Figure 1. Mobile Intel 945GM/GME/PM/GMS, 940GML Express Chipset and Intel 945GT Express Chipset Lead-Free Package Markings



§

Errata

1. LOCK to non-DRAM Memory Flag (register C8, bit 9) Is Getting Asserted

Problem: A CPU lock cycle request is unintentionally being recognized as a request to a non-system memory destination.

Implication: The GMCH may incorrectly flag an error for a valid lock cycle that targets DRAM. A system Error (SERR) may be generated if enabled by System BIOS.

Workaround: Do not enable or change default setting of ERRCMD[9] Bus 0 Device 0 Offset CAh (SERR reporting for Lock cycles to non-DRAM memory).

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

2. False Detection of a PCIe* Endpoint While Operating in PCIe Low Power Mode

Problem: Mobile Intel 945GM/GME/PM Express chipsets and the Intel 945GT Express chipset may falsely detect the presence of a PCIe endpoint while operating in PCIe low power mode.

- False detect may occur for systems supporting x1 only endpoints.
- False detect may occur on PCIe lanes 1 through 15 for a graphics endpoint when switching from x16 to x1.

Implication: System may become inoperable when an endpoint is operating in x1 mode. The scenario occurs because false detection of a PCIe endpoint occurs on one or more lanes resulting in the GMCH's PCIe interface erroneously entering and looping continuously in polling compliance. When an endpoint is operating in x1 mode, the scenario may occur at boot or during any subsequent attempt to retrain the link.

Workaround: For systems requiring x1 PCIe link operations:

1. Systems operating in x1 mode only: A BIOS workaround has been defined and is available.
2. Systems requiring run-time switching between x16 and x1 operation: a graphics driver workaround has been defined. Please contact your graphics controller vendor for driver status.
   Use the erratum title when contacting graphic's controller vendor for driver status.
3. For questions pertaining to the erratum or workaround please contact your Intel representative.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

3. System Memory Clocks Do Not Meet Certain JEDEC DDR2-667 DRAM Device Jitter Requirements

Problem: Excessive jitter observed on DDR2-667 (5-5-5) differential clocks. Intel has characterized the system memory clocks and system timing margins and shared the data with major DRAM suppliers. Intel has determined and major DRAM suppliers agree that this system clock jitter sighting should not cause memory-clock functionality or timing related issues providing all other DRAM related interface timings specification are fulfilled according to DDR2 Intel specification addendum (http://developer.intel.com/technology/memory/#Specs) and the JEDEC DDR2 DRAM specification.

Parameter	JEDEC Spec (ps)	(G)MCH (ps)
tJIT (per)	-125	-175
tJIT (cc)	-250	-325
tERR (2per)	-175	-215
tERR (4per)	-250	-275
tERR (5per)	-250	-275

Implication: None. No functional failures have been observed.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

4. Intermittent FAILURE to DETECT DVI Display Device during System Boot

Problem: It was observed that intermittently a DVI device attached would not be detected during system boot.

Implication: Intermittent failure to activate DVI display at boot time.

Workaround: BIOS workaround with special initialization of the shared PEG/SDVO port.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

5. DDR2 CLK to CKE Power-up Timing

Problem: During memory power-up and initialization, the timing between DDR2 clock stabilization to CKE going high is observed to be a minimum of 35 ns against the JEDEC spec of 200 µs.

Implication: None. No function failures have been observed. Intel has characterized timing and shared the data with major DRAM suppliers. Intel has determined, and major DRAM suppliers agree, that DRAM devices need < 35 ns. This erratum should not cause memory-clock functionality or timing related issues. Please refer to latest Intel DDR2 spec Addendum for power-up and initialization timing requirements available at http://developer.intel.com/technology/memory/#Specs.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

6. LVDS Panel Power Down Timing Violation during System Reset

Problem: During system reset, there is insufficient time for handshake between ICH and GMCH LVDS logic. As a result, timing from panel backlight enable going low to LVDS data going low (TX) and timing from LVDS data going low to panel VCC enable going low (T3) do not match the programmed values. Panel backlight enable (LBKLT_EN), panel Vcc enable (LVDD_EN) and LVDS data lines go low at the same time.

Implication: No system level issues have been observed.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

7. Hang/Blue Screen While Running 3D Workloads in Battery Mode

Problem: When running 3D graphics workloads for an extended period of time while on battery power, the system may hang or blue screen. Failure is observed only when the Intel® Dual-Frequency Graphics Technology (Intel® DFGT) feature is enabled.

Implication: System will require a reboot (Power Cycle).

Workaround: Intel DFGT is disabled in the Intel® Graphics Media Accelerator Driver (Intel® GMA Driver).

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

8. Screen-Corruption with Hardware VLD Enabled

Problem: When running a small percentage of DVDs, black block visual artifacts may be intermittently observed when using DVD software players that utilize hardware VLD. Artifact is mostly likely for scenes that are relatively static (i.e., no motion).

Implication: Black blocks within the DVD image may appear during playback of MPEG data.

Workaround: Hardware VLD is disabled in the Intel GMA Driver.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

9. No Display on Monitor After Resume from the Device Power-Down State with Intel® Smart 2D Display Technology (Intel® S2DDT) Enabled

Problem: When Intel Smart 2D Display Technology (Intel S2DDT) is enabled then the monitor may not resume its display when returning from Power Off state as defined by the operating system Control Panel / Power Options setting:

- Monitor Power Option is enabled.
- System is left idle and the system enters a power savings state.

Implication: The monitor may not resume from power off state when triggered by an appropriate user event (i.e., mouse movement), the system returns from idle.

Workaround: It is possible for the graphics driver to contain a workaround. Contact your Intel field representative for more details.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

10. CLK-CKE Hold Time Violation on DDR2

Problem: There exists a scenario during which the Clock Enable (CKE) signal has been observed to transition low to high on the rising edge of the clock.

- This may result in a JEDEC CKE hold time specification violation.

Implication: No known failures observed to date during Intel validation. There is a potential exposure to unexpected behavior on memory interface.

Workaround: BIOS workaround available.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*.

11. Power Saving Optimization Erratum

Problem: A Mobile Intel® 945 Express Chipset family errata related to a power savings optimization is causing a front side bus electrical issue.

- The feature shuts off output buffers when not being used.
- Power impact of disabling this feature is negligible, and Mobile® 945 Express chipset family meets all power targets.
- Affects All GMCH SKUs

Implication: System may fail to boot.

Workaround: A workaround is defined in the *Mobile Intel® 945 Express Chipset Family BIOS Specification Update* version 1.03 (set bit 13 and 29 = 0 FSBPMC3 40h).

Status: NoFix. For the steppings affected, see the *Summary Tables of Changes*.

12. Mobile Intel 945GM/945GME/945GMS/940GML/GU Express Chipset Internal Buffer Logic Erratum

Problem: A logic issue may cause an incorrect internal buffer flush to occur. Specific sequence of processor and internal graphics memory access must occur in a certain sequence for issue to occur.

Implication: System may hang. Issues have only been observed using specific customized stress test application. No productized SW application known to fail due to this issue.

Workaround: Workaround available in Intel Graphics driver for Windows* XP PV14.31.1.4864 or later and for Windows* Vista PV15.6.0.1322 or later.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

13. Mobile Intel 945 Express Chipset Family SMRAM D_CLS Bit Erratum

Problem: Data and stack residing in Extended SMRAM (TSEG/HSEG) are inaccessible when the D_CLS bit (Bus 0, Device 0, Function 0, Register 9Dh, Bit 5) is set.

Implication: May result in system hang.

Workaround: Refer to your Intel Representative for more details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

14. Mobile Intel® 945 Express Chipset Family Internal Race Condition between the Host and PCI Express Internal Clocks

Problem: The Mobile Intel 945 Express Chipset may experience an internal race condition between the host and PCI Express internal clocks and may experience a hang when the following conditions are met simultaneously:
1. When using a PCI Express endpoint (connected to MCH) that is generating at least 12 outstanding read requests to memory, with at least one of those requests setting the Relaxed Ordering attribute.

2. The CPU generates a downstream write burst (including a non-posted) to the PCI Express endpoint that stalls due to lack of PCI Express posted credits.
3. The MCH allows the Relaxed Order read completion to pass the posted memory.
Note: This has only been found in a synthetic testing environment

Implication: System may exhibit a hang with either of the three failing signatures:
1. MCH doesn't respond with completion to PCI Express-mem read (read completes on DDR2 I/F)
2. MCH responds with 2 completions (instead of 1) with duplicate tags in response to PCI Express-mem read (read also completes on DDR2 I/F)
3. CPU to PEG downstream write completes on FSB but never gets requested on PEG

Workaround: It is possible for system BIOS to contain a workaround. Contact your Intel field representative for more details.

Status: No Fix. For steppings affected, see the Summary Tables of Changes.

§

Specification Changes

1. Mobile Intel® 940GML Express Chipset Added Support for 200-MHz Display Clock

Section 1.6.3.

- 166 MHz Render clock and 200 MHz / 133 MHz Display clock at 1.05 V core voltage

§

Specification Clarifications

1. Clarification of TCO0 / TCO1 Default Value

The default values for the Thermal Calibration Offset registers are incorrect:

— Thermal Calibration Offset registers: TCO0 and TCO1 (MCHBAR+C92 & MCHBAR+CE2)

The TCO0 and TCO1 registers are automatically loaded with the TCO Fuse register values during power-up:

— TCO Fuse Registers: TCOF0 and TCOF1 (MCHBAR+CE6 & MCHBAR+C96)

After Power-up TCO0 and TCO1 = TCOF0 and TCOF1, respectively.

2. DMA Transfer Completion for Latency Sensitive Devices

It has been seen that DMA transfers on some latency-sensitive devices may incur completion delays during heavy external PCI Express* Graphics traffic to cacheable memory regions. These latency sensitive devices have been typically used in AC mode.

If such completion delays are encountered, a system BIOS configuration change is available that may allow a device to be serviced during heavy external PCI Express Graphics traffic. If such completion delays continue to be encountered an additional BIOS configuration change to disable C3 may be required to allow a device a device to be serviced during heavy external PCI Express Graphics traffic.

Please refer to your Intel Representative for more details.

§

Documentation Changes

1. Section 6.2.16 C0DRC0- Channel 0 DRAM Controller Mode 0 [6:4] Update

The following wording was added into the register description for C0DRC0[6:4]

MA[10] must be set to 0 to enable DQSB strobe complements.

For the remaining bit fields, refer to the JEDEC spec for DDR2

6:4	R/W 000 b	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. **000**: Post Reset state. When the MCH exits reset (power-up or otherwise), the mode select field is cleared to “000”. During any reset sequence, while power is applied and reset is active, the MCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During suspend, MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, MCH will be reset - which will clear this bit field to “000” and maintain CKE signals de-asserted. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. **001**: NOP Command Enable - All CPU cycles to DRAM result in a NOP command on the DRAM interface. **010**: All Banks Pre-charge Enable - All CPU cycles to DRAM result in an “all banks pre-charge” command on the DRAM interface. **011**: Mode Register Set Enable - All CPU cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. **MA[10] must be set to 0 to enable DQSB strobe complements, for the remaining bit fields, refer to the JEDEC spec for DDR2.** **100-101**: Reserved **110**: CBR Refresh Enable:In this mode all CPU cycles to DRAM result in a CBR cycle on the DRAM interface **111**: Normal operation

2. Replaced the Diagrams in Figure 37 and Figure 40

The Center Array view has been changed from Top View to bottom view.

Figure 37. Mobile Intel 945GMS Express Chipset Package FCBGA

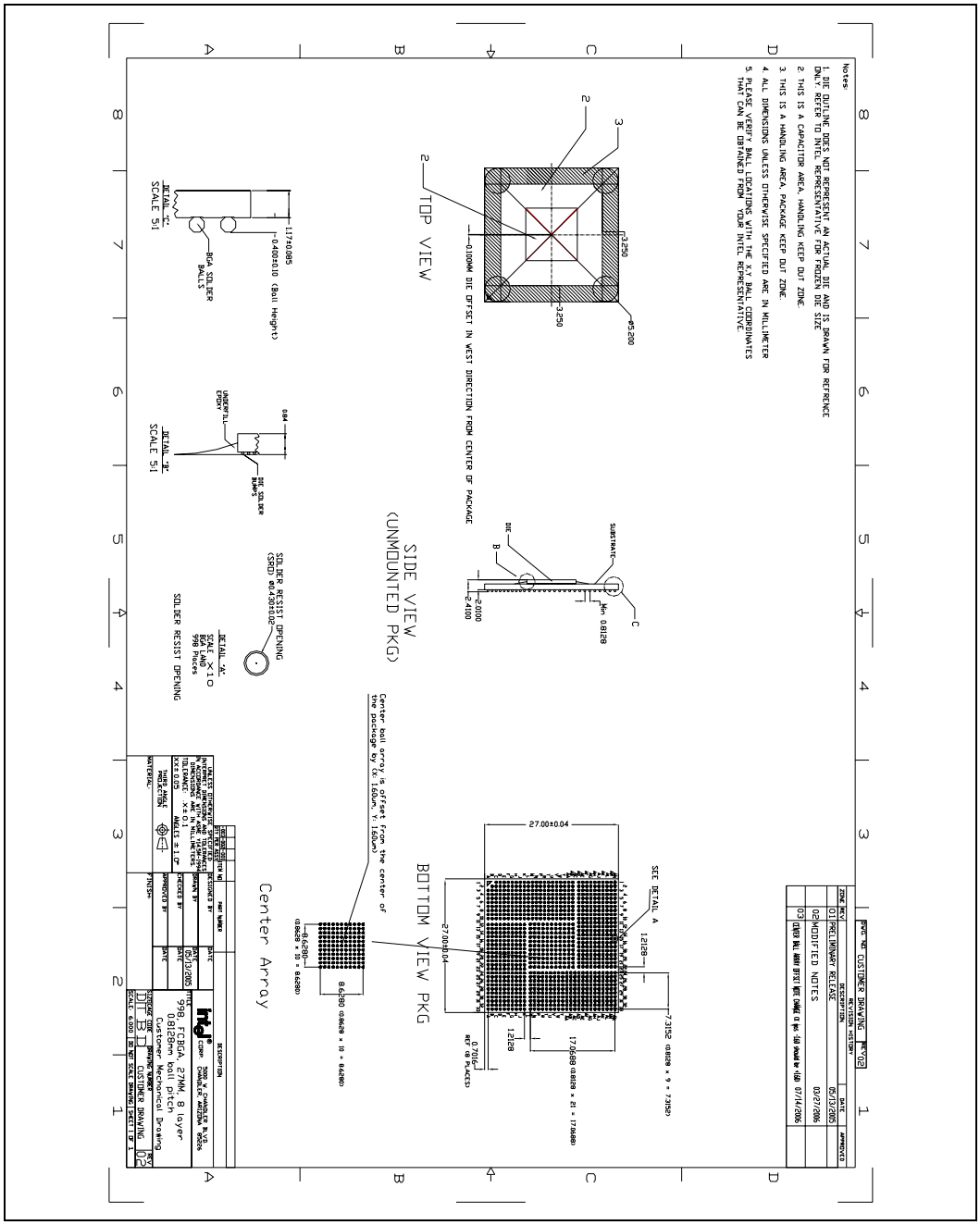
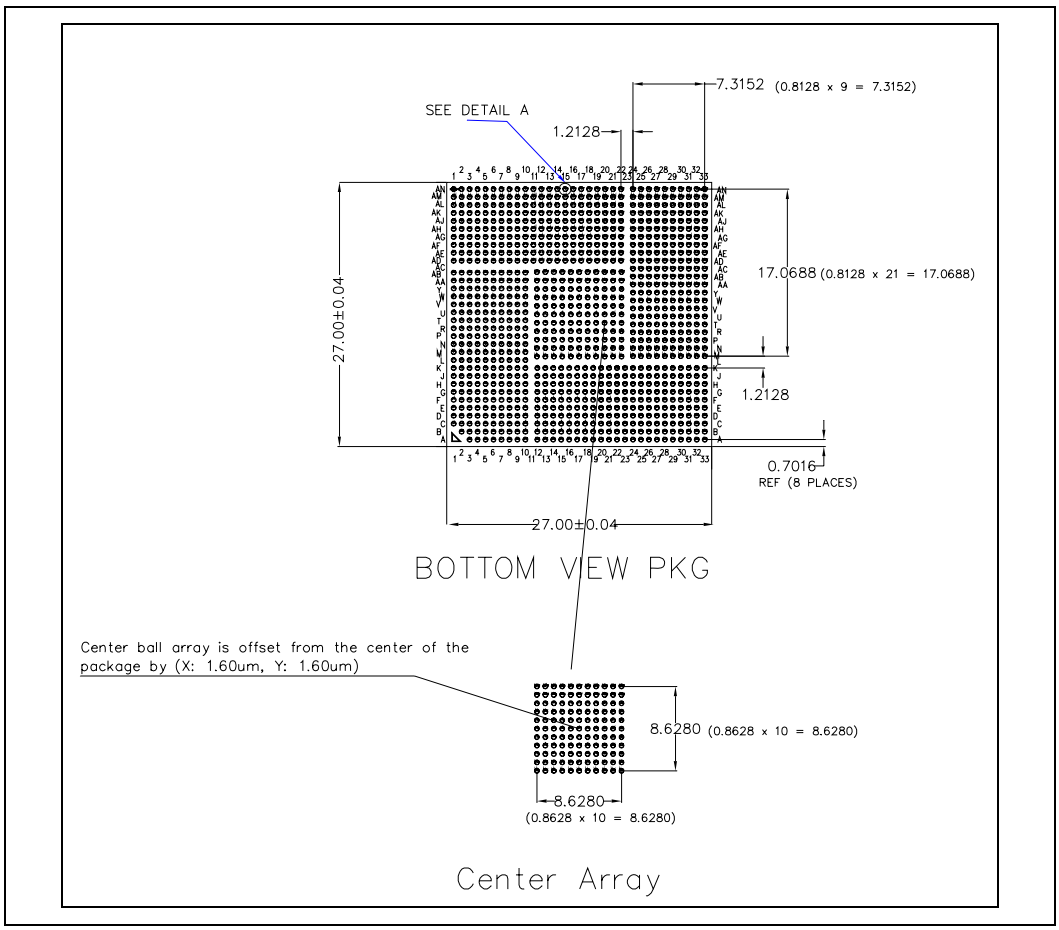


Figure 40. Mobile Intel 945GMS Express Chipset Package FCBGA (Bottom View)

The Center Array view was incorrectly shown from the Top. This has been changed to bottom view. The offset information has also been accordingly updated.



§